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09/517,345	03/02/2000	Sidney Larry Anderson	15114-052310	4253

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/517,345	Applicant(s) Anderson et al
	Examiner Nitin Parekh	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Nov 13, 2002*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-25 and 49-66* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-25 and 49-66* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *? and 1?*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-25 and 49-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller (US Pat. 5866949) in view of Zenner et al (US Pat. 6246010), Welkowsky et al (US Pat. 5160560) and the admitted prior art (APA).

Regarding claim 1, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a silicon die (52 in Fig. 3B/3A) having a first thickness
- a metallized polymer layer/flexible dielectric tape substrate (59/60 in Fig. 3B/3A; Col. 7, line 30) having a first/top side and a second/bottom side, and
- a transition medium/support structure (50 in Fig. 3B/3A) disposed between the silicon die and the first side of the metallized polymer layer where the transition medium/support structure has a second thickness

(Fig. 3B/3A; Col. 8, line 12- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Schueller discloses using a single transition medium/support structure having a second thickness of 100-250 microns (Col. 9, line 49) or using a plurality of those (Col. 11, line 12) but fails to specify the first thickness of the silicon die being less than the second thickness.

Zenner et al teach using a high density/thin package having a die thickness of about less than 100 microns or preferably less than 20 microns and a package thickness of about 275 microns (Col. 2, line 15-22; Col. 3, line 55) to reduce the total volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

Welkowsky et al teach using thin chips/wafers for a variety of semiconductor applications where the chip thicknesses are about 30 microns, 5 mils, etc. (Col. 7, line 20-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first thickness of the silicon die with a smaller thickness than the second thickness of transition medium so that the thermal stress can be reduced and the functionality/reliability of the package can be improved using Zenner et al and Welkowsky et al's chip designs in Schueller.

Regarding claim 2, Schueller discloses the transition medium/support structure comprising a single or multilayered structure including conventional conductive/non-conductive material such as ceramic, metal, PCB or a combination of metal and non-metal/epoxy PCB material (Col. 9, line 58; Col. 10, line 27; Col. 11, line 12). Furthermore, Schueller discloses selecting the transition medium/support structure to provide various functions such as improved rigidity/strength (Col. 9, line 52), thermal dissipation (Col. 9, line 10), etc. so that the thermal stress and defects such as fracture, cracking, etc. can be reduced (Col. 6-10).

Regarding claim 3, Schueller further discloses encapsulating the silicon die and the transition medium with a conventional plastic encapsulant/mold cap, the die being coupled to the transition medium and being disposed near the middle of the package (Col. 8, line 40; Fig. 3B) but fails to specify the encapsulant and adhesive having a thermal coefficient of expansion (CTE) approximately in a range of 7-15 x $10^{-6}/^{0}$C and 58 x $10^{-6}/^{0}$C respectively.

The conventional encapsulant and adhesives used in chip packaging and encapsulation technology art have thermal coefficient of expansion (CTE) range of 7-15 x $10^{-6}/^{0}$C and approximately 58 x $10^{-6}/^{0}$C respectively (Table 2- admitted prior art).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plastic encapsulant having approximate

CTE range of 7-17 x $10^{-6}/^{0}C$ so that the thermal stress can be reduced in Schueller's package in view of Zenner et al, Welkowsky et al and APA.

Regarding claim 4, Schueller further discloses the transition medium/support structure being made of conventional nonconductive epoxy/PCB/FR-4 type material (Col. 10, line 18-27). Furthermore, It is conventional in chip packaging art to use such nonconductive material/packaging substrates as epoxy, molded plastic, FR-4/5, BT resin, etc.

Regarding claim 5, Schueller fails to specify the range of CTE for the transition medium being 10-17 x $10^{-6}/^{0}C$.

However, as explained above for claim 4, Schueller discloses the transition medium/support structure being made of PCB/FR-4 type material and further discloses conventional BGA packages having an adhesive and an elastomer being used as a transition medium (224 in Fig. 2 and 10 in Fig. 1 respectively; Col. 5 and 6). Furthermore, such conventional material/substrates as epoxy, molded plastic, FR-4/5, BT resin, etc. have typical CTE in the range of 7-17 x $10^{-6}/^{0}C$ (see admitted prior art-Table 2).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the transition medium having the CTE range of

7-17 x $10^{-6}/^{0}C$ so that the thermal stress can be reduced in Schueller's package in view of Zenner et al, Welkowsky et al and APA.

Regarding claim 6, as explained above for claims 1 and 2, Schueller in view of Zenner et al, Welkowsky et al and APA teaches using the transition medium to reduce stress and fracture damage to the die.

Regarding claim 7, as explained above for claims 1 and 3, Schueller discloses the die being disposed near the middle of a package having a thickness where the package thickness is defined by the thickness of the metallized polymer layer/tape and that of the plastic encapsulant/mold cap (Col. 8, line 40; Fig. 3B)

Regarding claim 8, Schueller fails to specify the dimensions such as the thickness of the package and die being 0.06 inches and 6 mils respectively or the cross-sectional area/volume of the die being larger/smaller than that of the transition medium respectively.

As explained above for claim 1, Schueller in view of Zenner et al, Welkowsky et al and APA teaches using the die and package thickness range of about 30-100 microns or 5 mils and 275 microns or 0.01 inches respectively. Furthermore, determination of parameters such as a package/die thickness and thickness ratio, die

area, area ratio of various components, volume, weight, respective values/ranges, relative position and an arrangement of various components within the package, material properties of components (substrate, adhesive/mold, etc.) including CTE, modulus, etc. in the chip packaging and encapsulation technology art are a subject of routine experimentation and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress distribution.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the thickness of the package and the die to be less than approximately 0.060 inches and 6 mils respectively and the area/volume of the die being less than, equal or larger than that of the transition medium so that the desired thermal/mechanical stress can be reduced and the and the reliability of the package can be improved using Zenner et al and Welkowsky et al and APA's chip designs in Schueller.

Regarding claim 9, as explained above for claims 1 and 8, Schueller in view of Zenner et al, Welkowsky et al and APA teaches selecting the die thickness being less than approximately 6 mils.

Regarding claim 10, Schueller discloses coupling of the silicon die to the transition medium using an adhesive (Fig. 3B; Layer 64).

Regarding claim 11, as explained above for claims 1, 3 and 10, Schueller in view of Zenner et al, Welkowsky et al and APA teaches selecting the adhesive having a CTE of approximately 58 x $10^{-6}/^{0}C$.

Regarding claim 12, as explained above for claim 1, Schueller further discloses the metallized polymer layer/flexible dielectric tape having conventional dielectric and conductive layers (60 and 59 respectively in Fig. 3B; Col. 7).

Regarding claim 13, as explained above for claims 1 and 12, Schueller further discloses using solder balls being mounted to the second side of the metallized polymer layer, the solder balls electrically contacting the etched circuit in a conductive layer of the tape carrier (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6).

Regarding claim 14, as explained above for claims 1, 12 and 13, Schueller further discloses using the solder balls electrically connecting the package to a PCB (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6).

Regarding claim 15, as explained above for claims 1, 12 and 13, Schueller further discloses using the solder balls being arranged in a grid fashion under the position of the die (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6).

Regarding claim 16, as explained above for claims 1, 2 and 8, Schueller in view of Zenner et al, Welkowsky et al and APA teaches selecting the die having a cross-sectional area being substantially less than or equal to that of the rigid transition medium.

Regarding claim 17, as explained above for claims 1, 2 and 8, Schueller in view of Zenner et al, Welkowsky et al and APA teaches selecting the die having a cross-sectional area being larger than that of the transition medium.

Regarding claim 18, as explained above for claim 1, Schueller discloses the package being a BGA package.

Regarding claim 19, as explained above for claims 1, 2 and 8, Schueller in view of Zenner et al, Welkowsky et al and APA teaches selecting the die having a volume being less than that of the rigid transition medium.

Regarding claim 20, as explained above for claims 1, 3 and 7, Schueller in view of Zenner et al, Welkowsky et al and APA teaches having the die being disposed near the middle of a package thickness.

Regarding claim 21, as explained above for claims 1, 3-5 and 7, Schueller in view of Zenner et al, Welkowsky et al and APA teaches selecting the mold cap/encapsulant and transition medium having a similar value/range of the CTE.

Regarding claim 22, as explained above for claims 1 and 10, Schueller discloses mounting the silicon die to the transition medium using an adhesive (Fig. 3B; Layer 64).

Regarding claim 23, as explained above for claims 1, 4, 10, 20 and 22, Schueller discloses the transition medium/support structure comprising a layer/second layer of adhesive, elastomer, epoxy/BT resin/FR-4 or 5 resin compound.

Regarding claim 24, as explained above for claims 1 and 12, Schueller discloses the metallized polymer layer being a tape carrier.

Regarding claim 25, as explained above for claims 1, 3 and 20-24, Schueller further discloses using the first and second adhesive layers (56/64 in Fig. 3B) having

respective thickness/CTE disposed on the tape carrier and the transition medium respectively (Fig. 3B; Col. 9, line 65; Col. 8, line 12- Col. 10, line 36) and the adhesive layers having thickness in a range of 25-50 microns (Col. 10, line 18) which is less than that of the transition medium/support which is 100-250 microns (Col. 9, line 49) but fails to specify the thickness of the adhesive, transition medium and die being nearly equivalent or same as half of the package thickness to reduce the thermal stress.

As explained above for claims 1, 3, 8 and 21, Schueller in view of Zenner et al and Welkowsky et al teach selecting the package/die dimensions and material such that the thickness of the adhesive, transition medium and die being nearly equivalent or same as half of the package thickness and the transition medium and the mold cap being of approximately same CTE so that the thermal stress during thermal cycling can be reduced.

Regarding claim 49, as explained above for claims 1-19, 20 and 25, Schueller further discloses an integrated circuit (IC)/Ball Grid Array (BGA) package having only a single or multiple IC dice, the package comprising

- an IC die (52 in Fig. 3A) having a front side, backside and a first thickness between the front and back sides, where the bonding pads (Col. 8, line 25) are formed on the front side

- a metallized polymer layer/tape substrate (58/59/60 in Fig. 3A) having a first side and a second side wherein the bonding pads are electrically coupled to the features/patterns (59 in Fig. 3A) of the metallized polymer layer/tape using bonding wires (82A in Fig. 3A)

- a transition medium/support structure between the IC die and the metallized polymer layer (50A in Fig. 3A) having only an adhesive layer (64A in Fig. 3A) between the two where the transition medium/support structure has a second thickness, the second thickness being relatively uniform and none of the bonding pads being electrically coupled to the transition medium

- the backside of the IC die faces toward the transition medium and the front side of the IC die faces away from the metallized polymer layer/tape

- the IC die, metallized polymer layer/tape and transition medium are parallel planes, and

- solder balls (54 in Fig. 3A) below the metallized polymer layer/tape and the IC die electrically coupled to the bonding pads

(Fig. 3A; Col. 8, line 24; Col. 7, line 3- Col.1, line 12).

As explained above for claim 1, Schueller in view of Zenner et al, Welkowsky et al ans APA teaches using the second thickness being greater than the first thickness.

Regarding claim 50, as explained above for claims 1 and 49, Schueller discloses the front side of the die being faced away from the metallized polymer layer/tape.

Regarding claim 51, as explained above for claims 1 and 49, Schueller discloses the IC die, metallized polymer layer/tape and transition medium being three parallel planes.

Regarding claim 52, as explained above for claims 1 and 49, Schueller discloses the transition medium/support structure having a single/relatively uniform thickness.

Regarding claim 53, as explained above for claims 1 and 49, Schueller discloses the package accommodating only a single IC die.

Regarding claim 54, as explained above for claims 1 and 49, Schueller discloses the bonding pads being electrically coupled to the features/patterns of the metallized polymer layer/tape using bonding wires.

Regarding claim 55, as explained above for claims 1 and 4, Schueller further discloses using the transition medium/support comprising a single or multilayered structure including non-polymer material, ceramic or a combination of metal and non-metal/epoxy PCB material (Col. 9, line 58; Col. 10, line 27; Col. 11, line 12).

Regarding claim 56, as explained above for claims 1 and 49, Schueller discloses none of the bonding pads being electrically coupled to the transition medium.

Regarding claim 57, as explained above for claims 1 and 49, Schueller discloses having only an adhesive layer between the transition medium/support structure and IC die.

Regarding claim 58, as explained above for claims 1 and 49, Schueller discloses the back side of the die facing toward the transition medium.

Regarding claim 59, as explained above for claims 1 and 49, Schueller discloses the IC package being a BGA package.

Regarding claim 60, as explained above for claims 1, 5 and 49, Schueller in view of Zenner et al, Welkowsky et al and APA teaches selecting the transition medium having the CTE range of 7-17 x $10^{-6}/^{0}C$.

Regarding claim 61, as explained above for claims 1 and 49, Schueller discloses using the solder balls below the metallized polymer layer/tape and the IC die electrically coupled to the bonding pads.

Regarding claim 62, as explained above for claims 1 and 49, Schueller in view of Zenner et al, Welkowsky et al and APA teaches selecting the substrate, silicon die and the transition medium where the thickness of the transition medium is greater than that of the die.

Regarding claim 63, as explained above for claims 1, 25 and 49, Schueller in view of Zenner et al, Welkowsky et al and APA teaches using the first and second adhesive layers being positioned between the transition medium and substrate/die respectively.

Regarding claim 64, as explained above for claims 1, 7 and 20, Schueller in view of Zenner et al, Welkowsky et al and APA teaches positioning the die approximately at the middle of the package thickness.

Regarding claim 65, as explained above for claims 1 and 4, Schueller in view of Zenner et al, Welkowsky et al and APA teaches using the transition medium comprising a mold material, BT resin/epoxy, FR-4 or FR-5 compound.

Regarding claim 66, as explained above for claims 1 and 5, Schueller in view of Zenner et al, Welkowsky et al and APA teaches using the transition medium having the CTE range of 7-17 x $10^{-6}/^{0}C$.

Response to Arguments

3. Applicant's arguments filed on 11-13-02 have been fully considered but they are not persuasive.

A. Applicant contends that Figures in Schueller show the IC package/tape carrier having the transition medium of a greater thickness than the silicon die and there is no motivation to combine Schueller with Zenner et al.

However, as explained above, Fig. 3A/B in Schueller show the IC package structure where various components such as transition medium, flexible tape/carrier, adhesive layer, mold/encapsulant, die, bonding wires, solder balls, etc. are shown with respect to their layout/placement and an arrangement within the package. The Figures in Schueller do not indicate/represent the numerical values of the dimensions/thickness for the die or the molded package.

Zenner et al teach using a thin package (about 275 microns in thickness) having a flexible substrate and using a silicon die having a lower thickness (about less than about 20 microns) than that of the support medium/structure (Fig. 1 and 2; Col. 3 and 4) so that the total volume of the package can be reduced and the functionality/reliability can be improved by reducing the thermal expansion mismatch and thermal stress (Col. 2, line 15-22; Col. 4, line 55- Col. 5, line 20). Therefore, Zenner et al's chip design/structure is applied to Schueller's IC package to reduce the thermal stress.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by Facsimile transmission. Papers should be faxed to Art Unit via Tech Center 2800 fax center located in Crystal Plaza 4, Room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh at (703) 305-3410. The examiner can normally be reached on Monday-Friday from 08:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

01-23-03

Tom Thomas

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